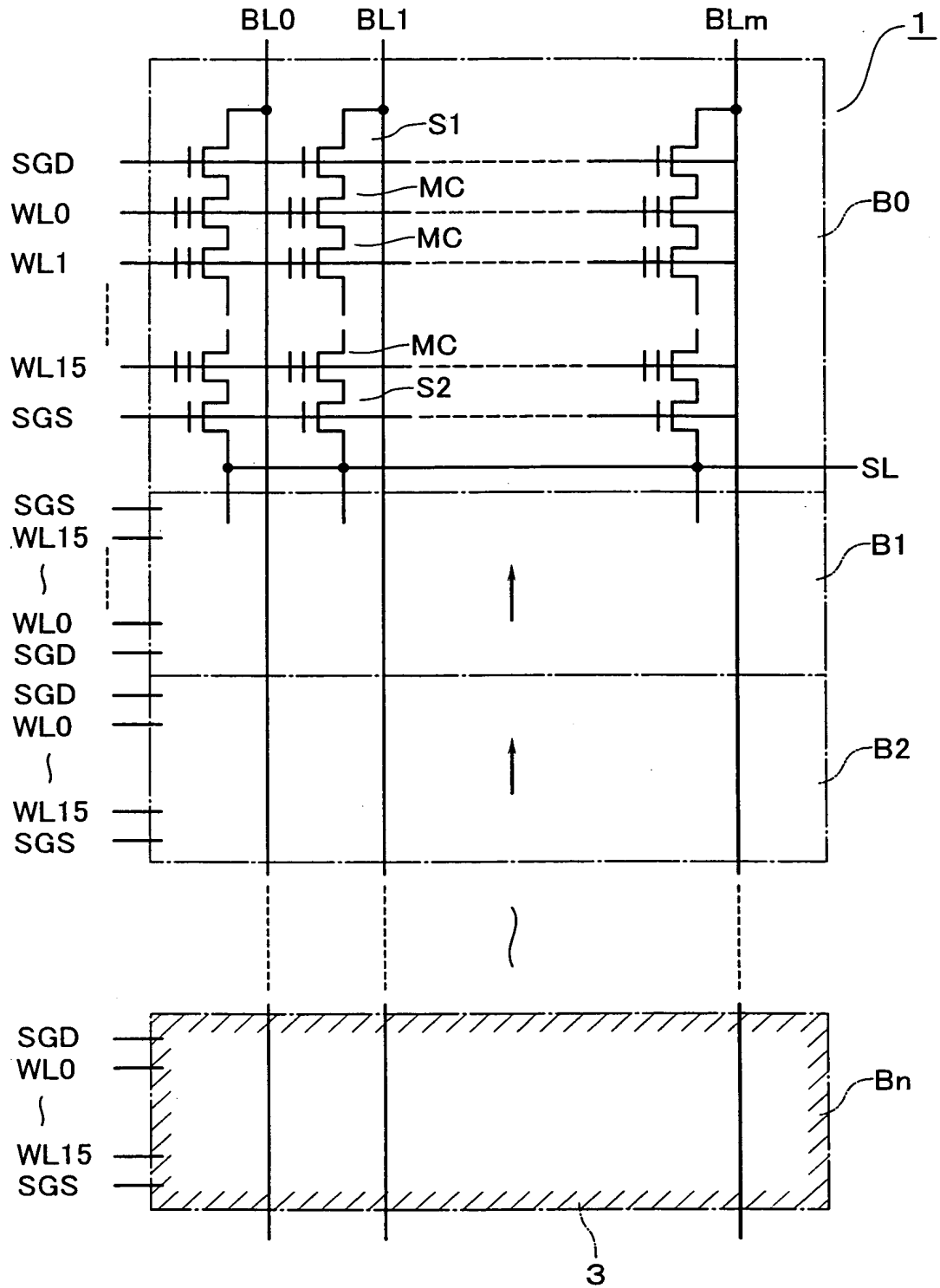


FIG. 2



**FIG.3B**

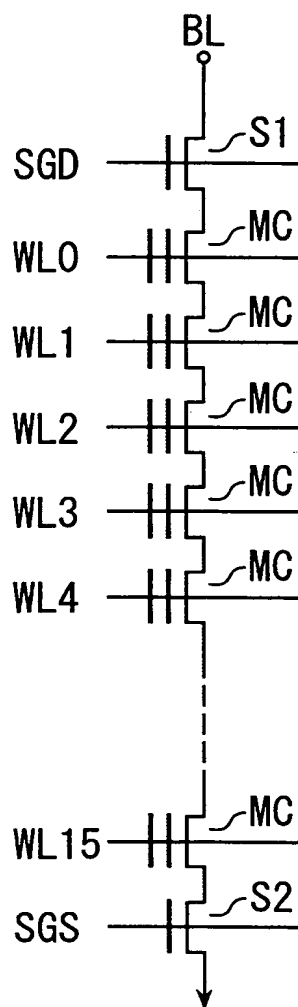


FIG.4A

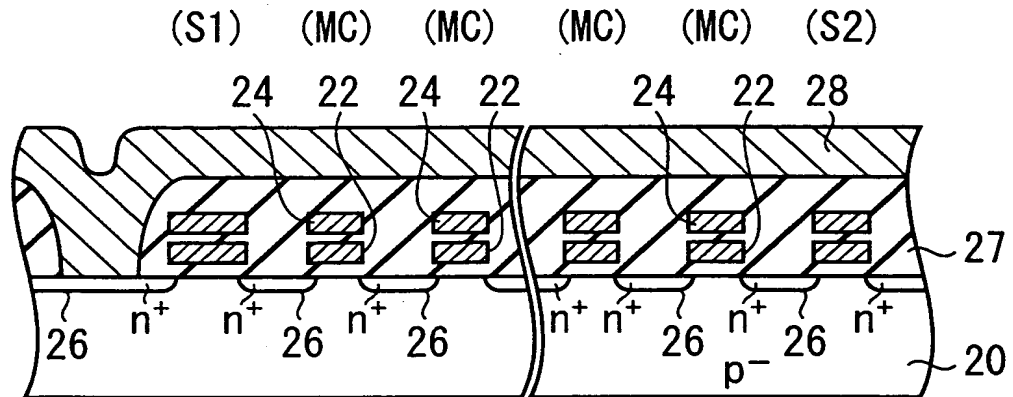


FIG.4B

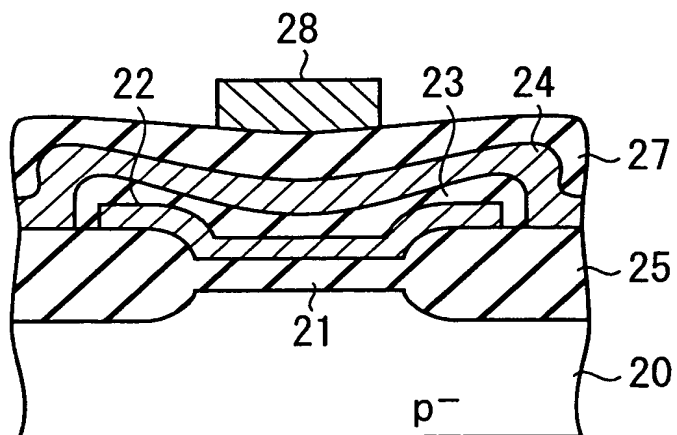


FIG.5

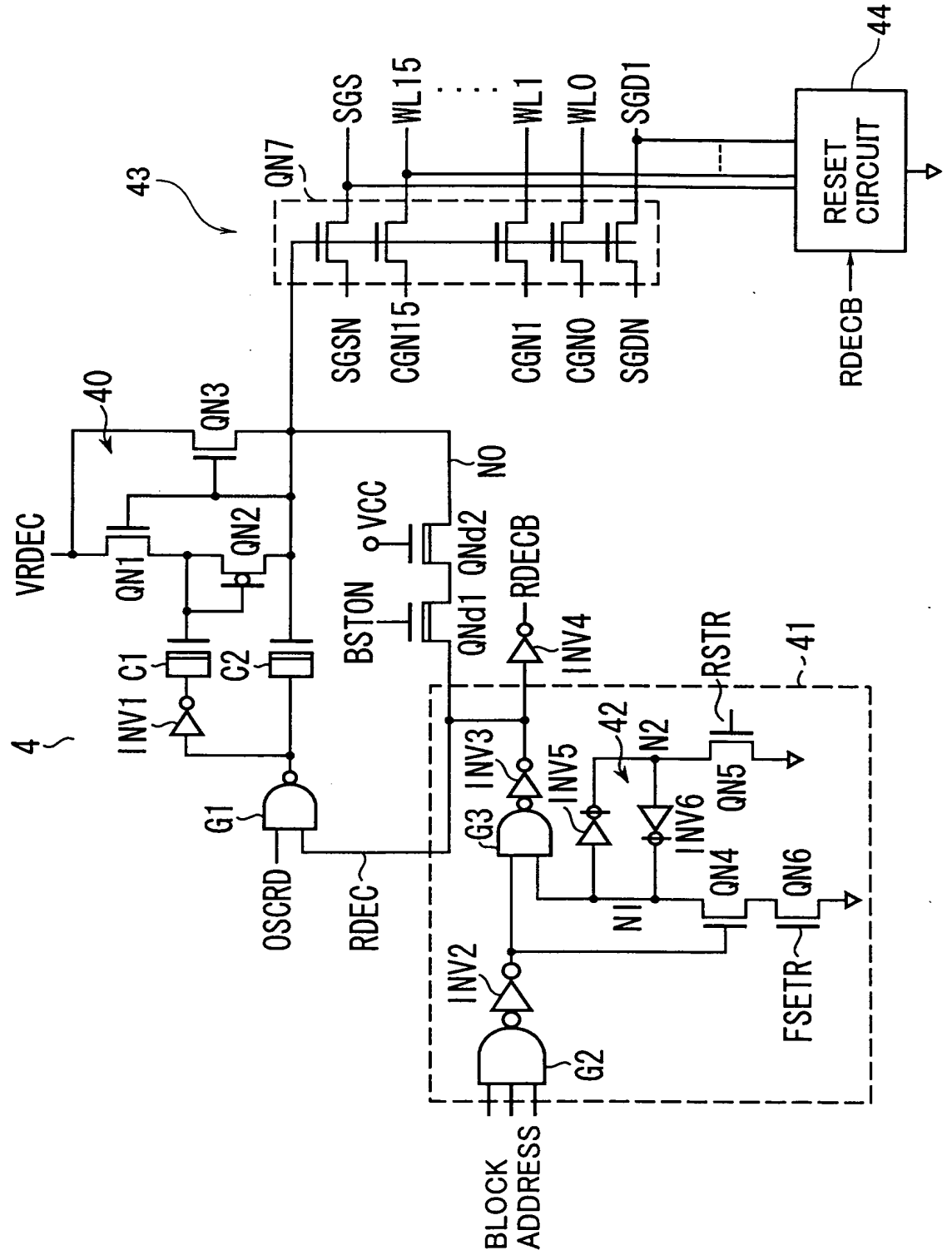
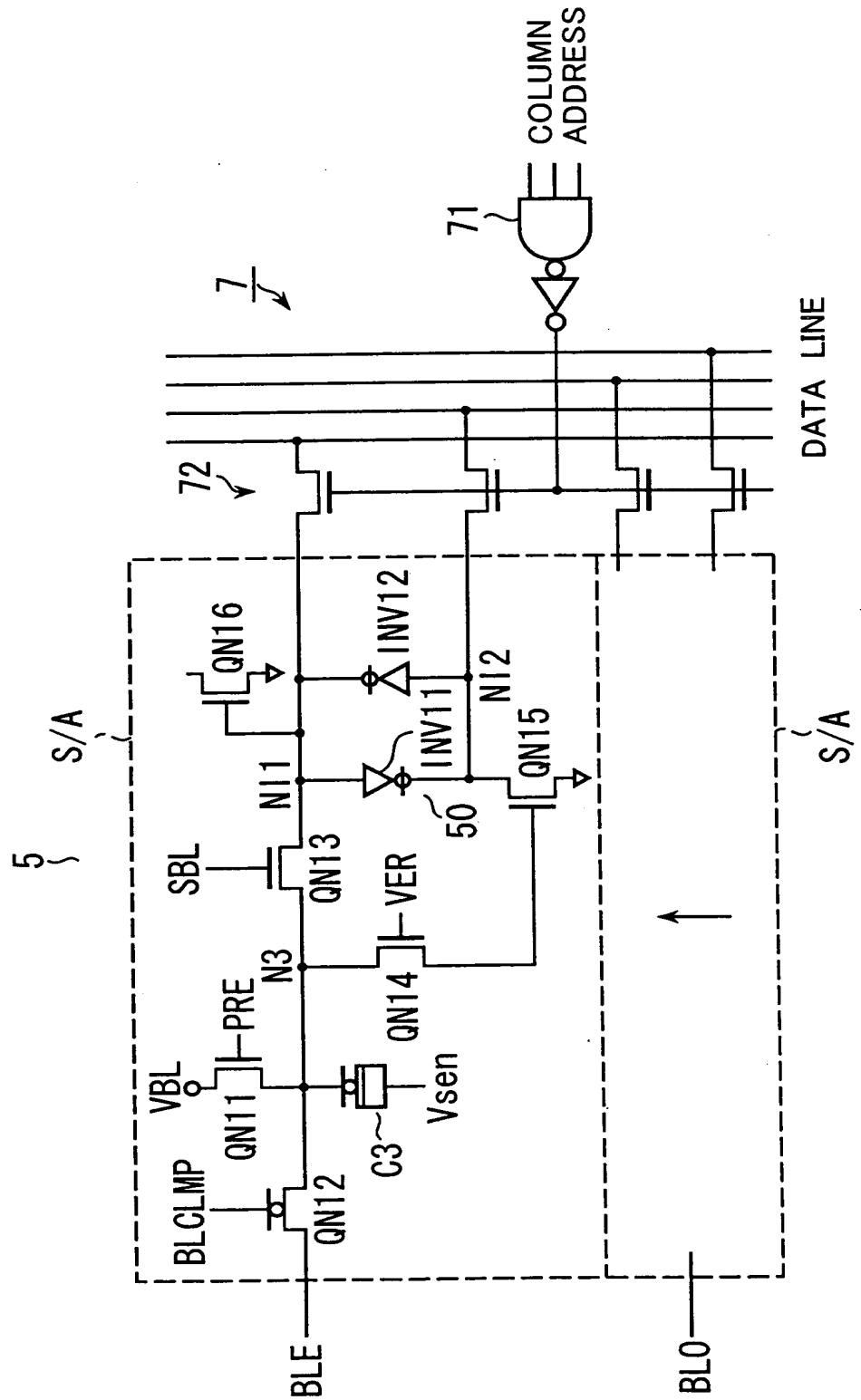
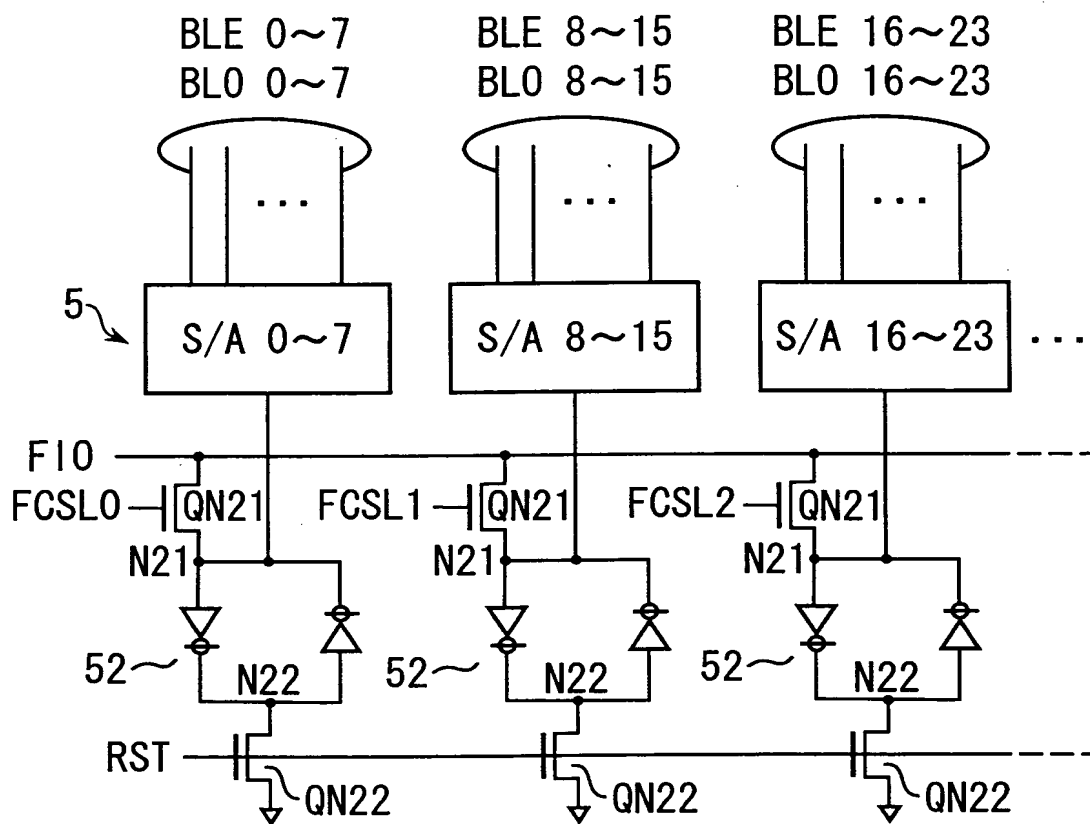


FIG.6





MEMORY ARRAY 1

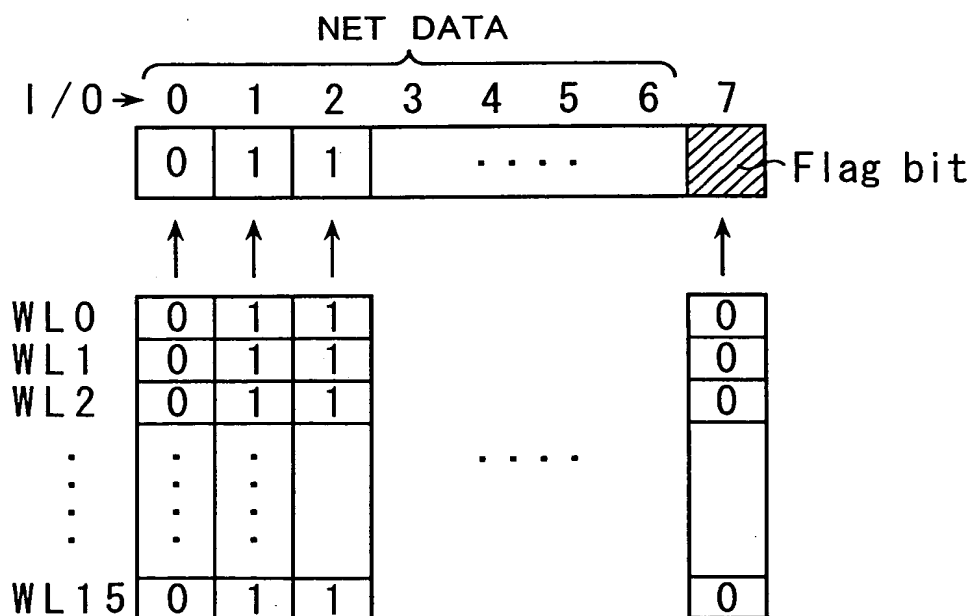




FIG.10A

EVEN PAGE (DEFECTIVE COLUMN ADDRESS)

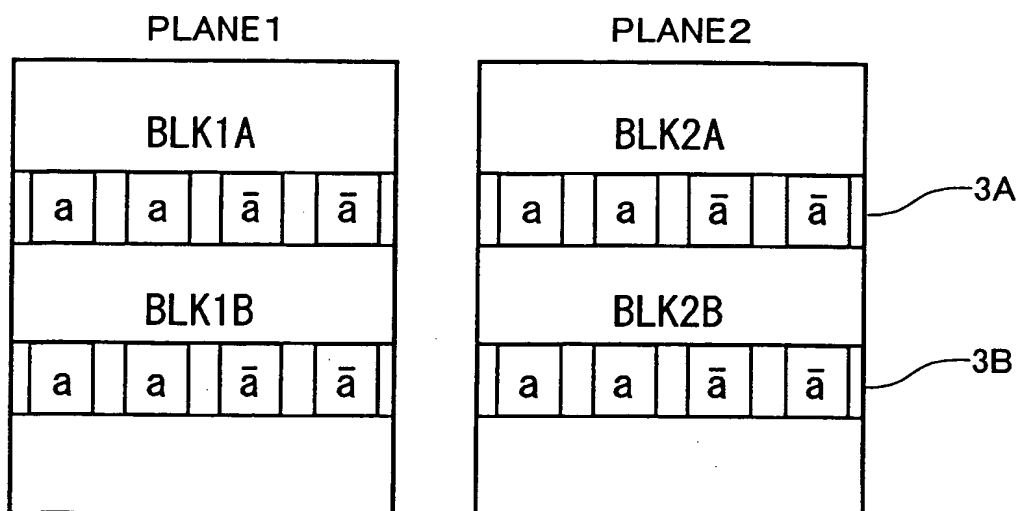


FIG.10B

ODD PAGE (DEFECTIVE BLOCK ADDRESS+OPTION DATA)

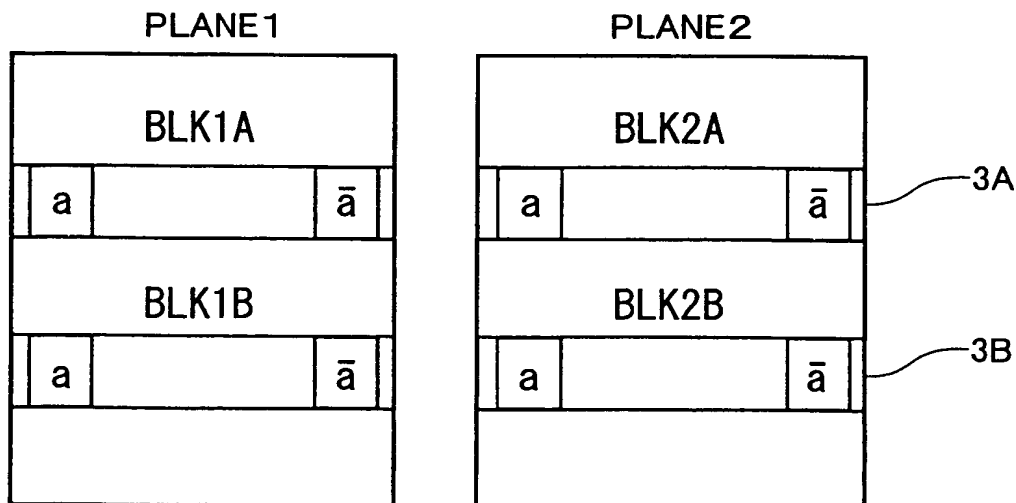


FIG.11

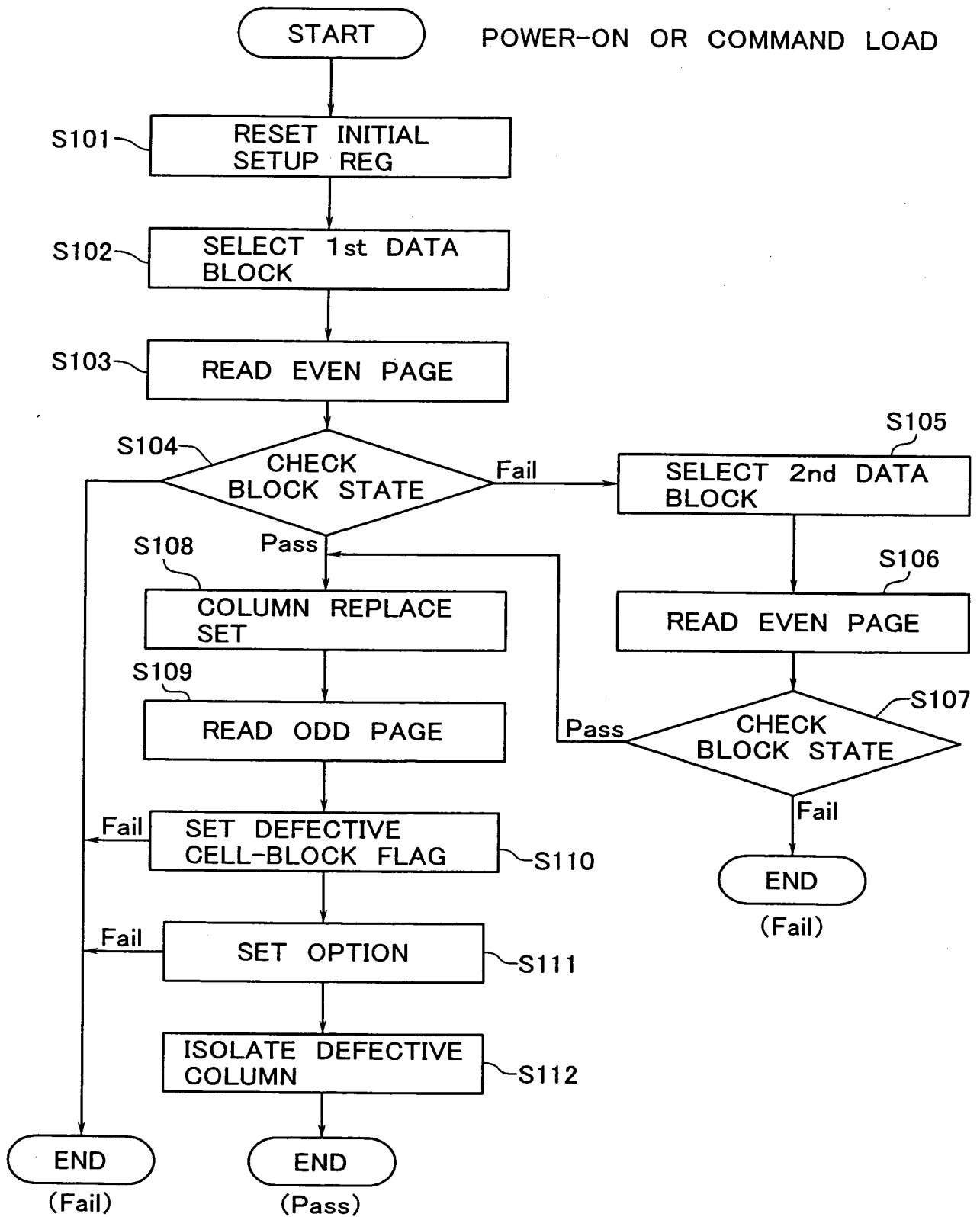


FIG.12

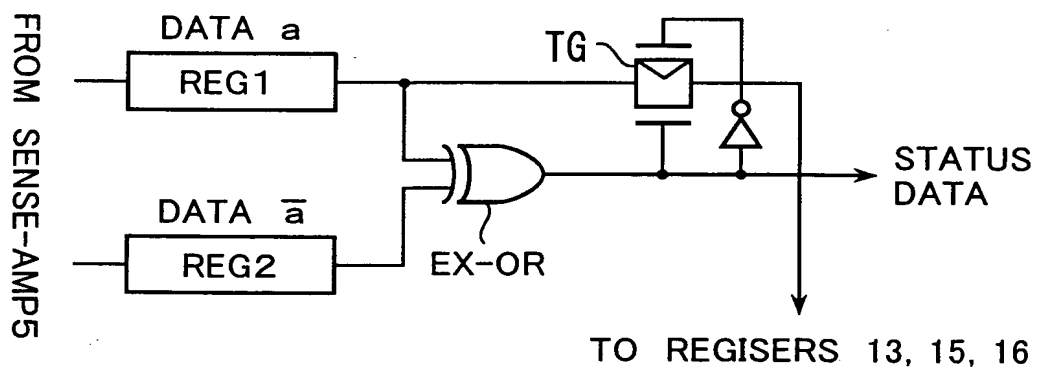


FIG.13

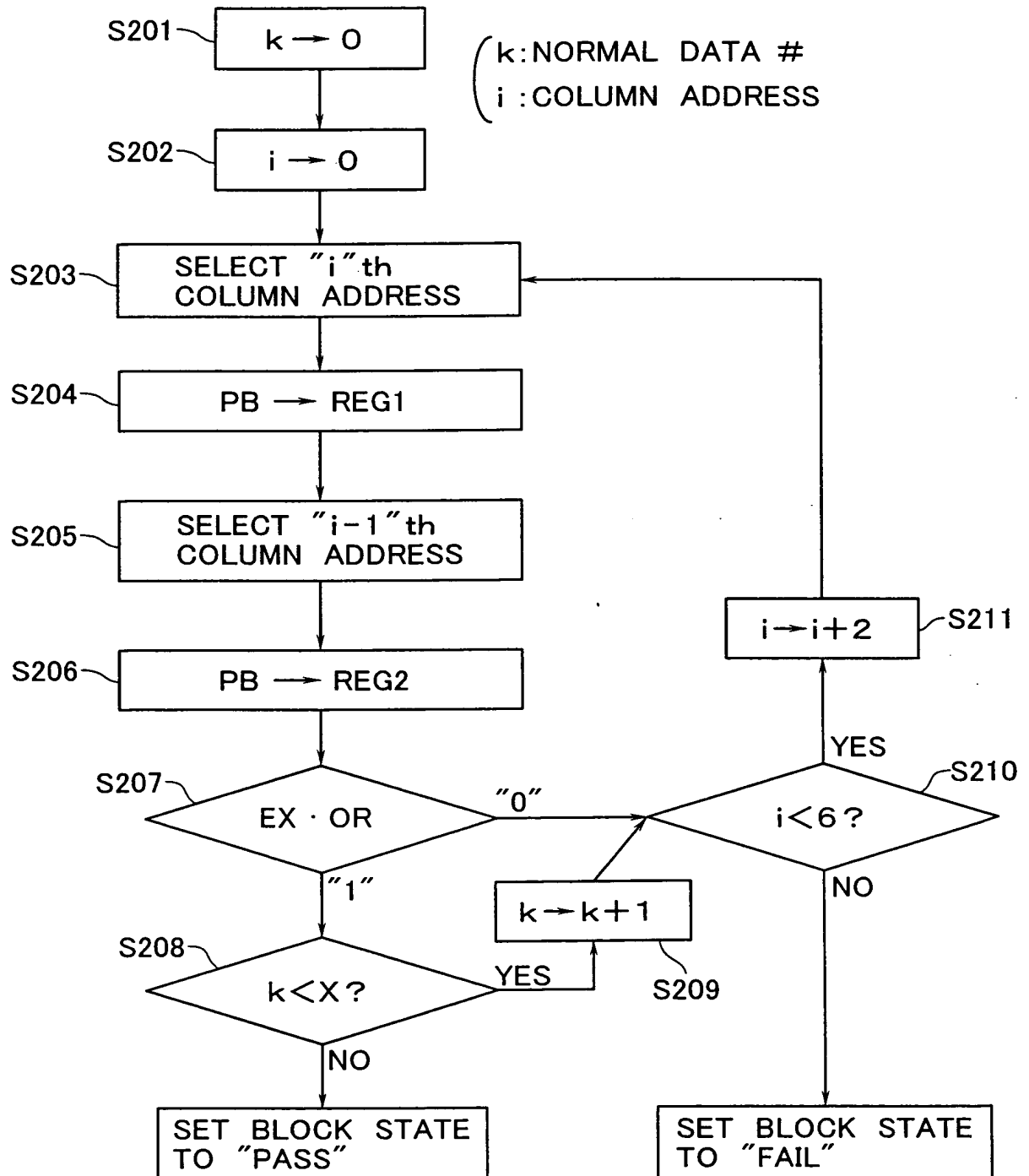
BLOCK STATE CHECH AT S104 & S107

FIG.14

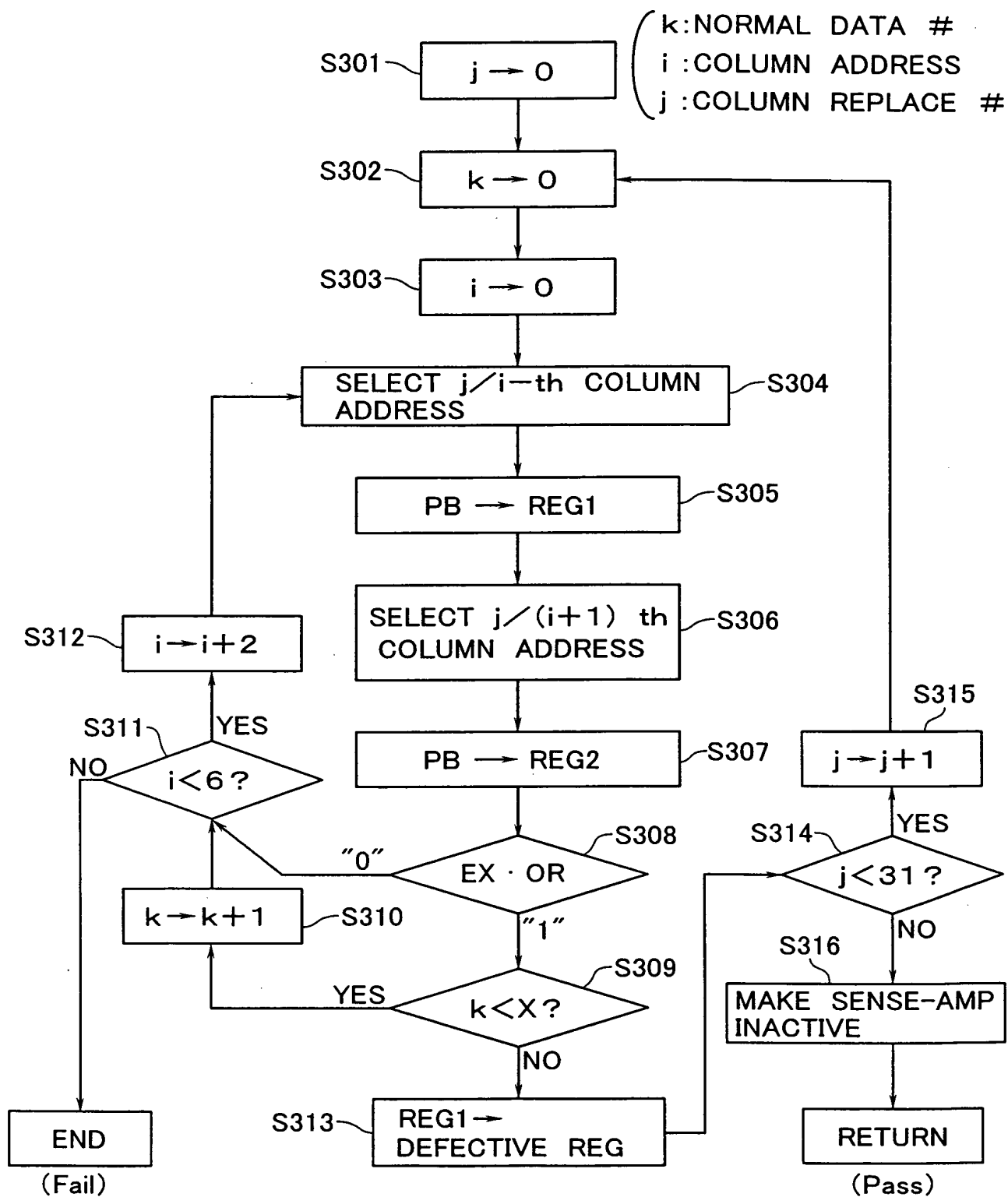
COLUMN REPLACE/SETTING AT S108

FIG.15

DEFECTIVE CELL-BLOCK  
FLAG SETUP AT S110  
OPTION SETUP AT S111

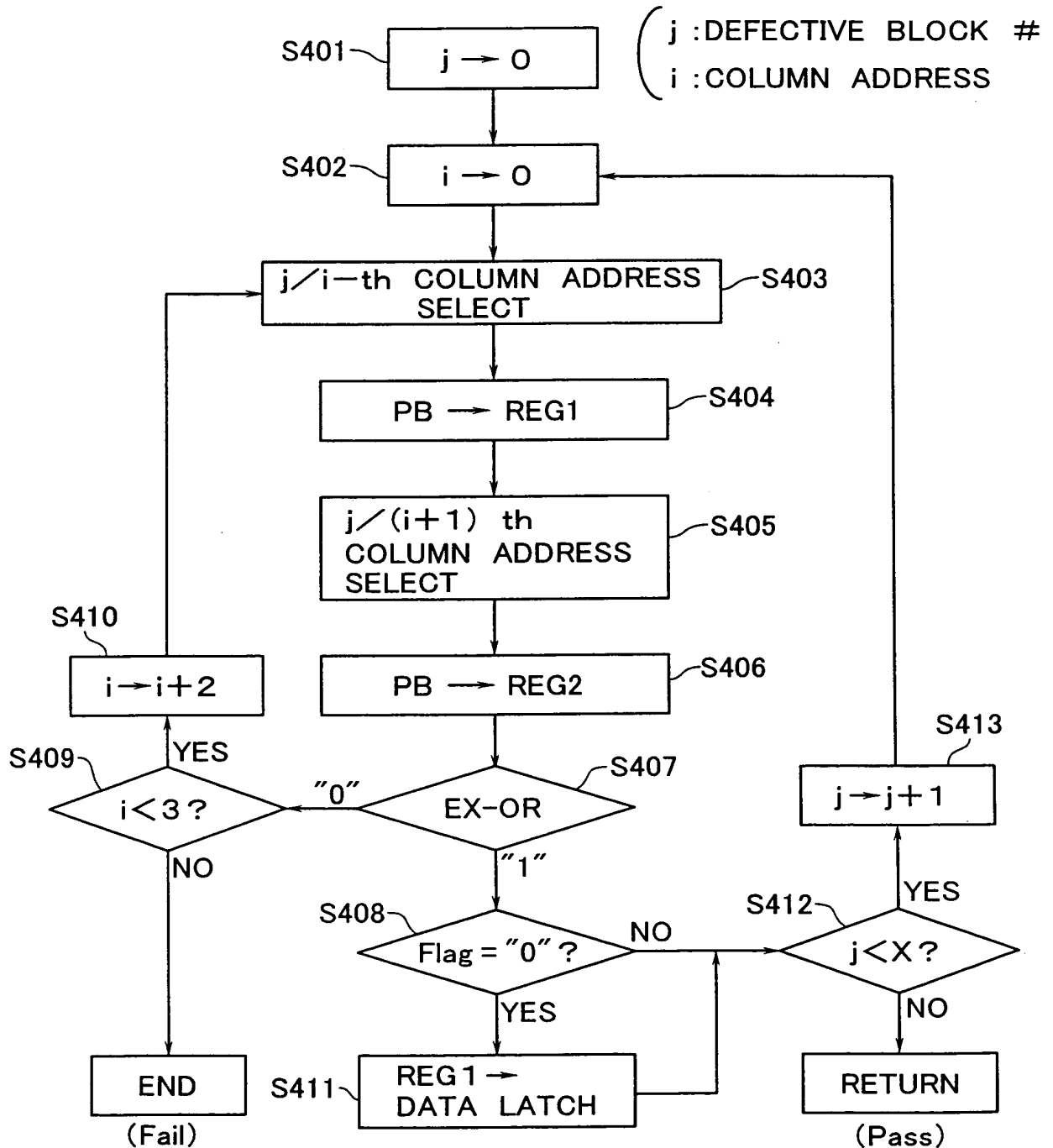


FIG.16

INITIAL SETUP DATA PROGRAMMING  
(WITHOUT AUTOMATIC TEST)

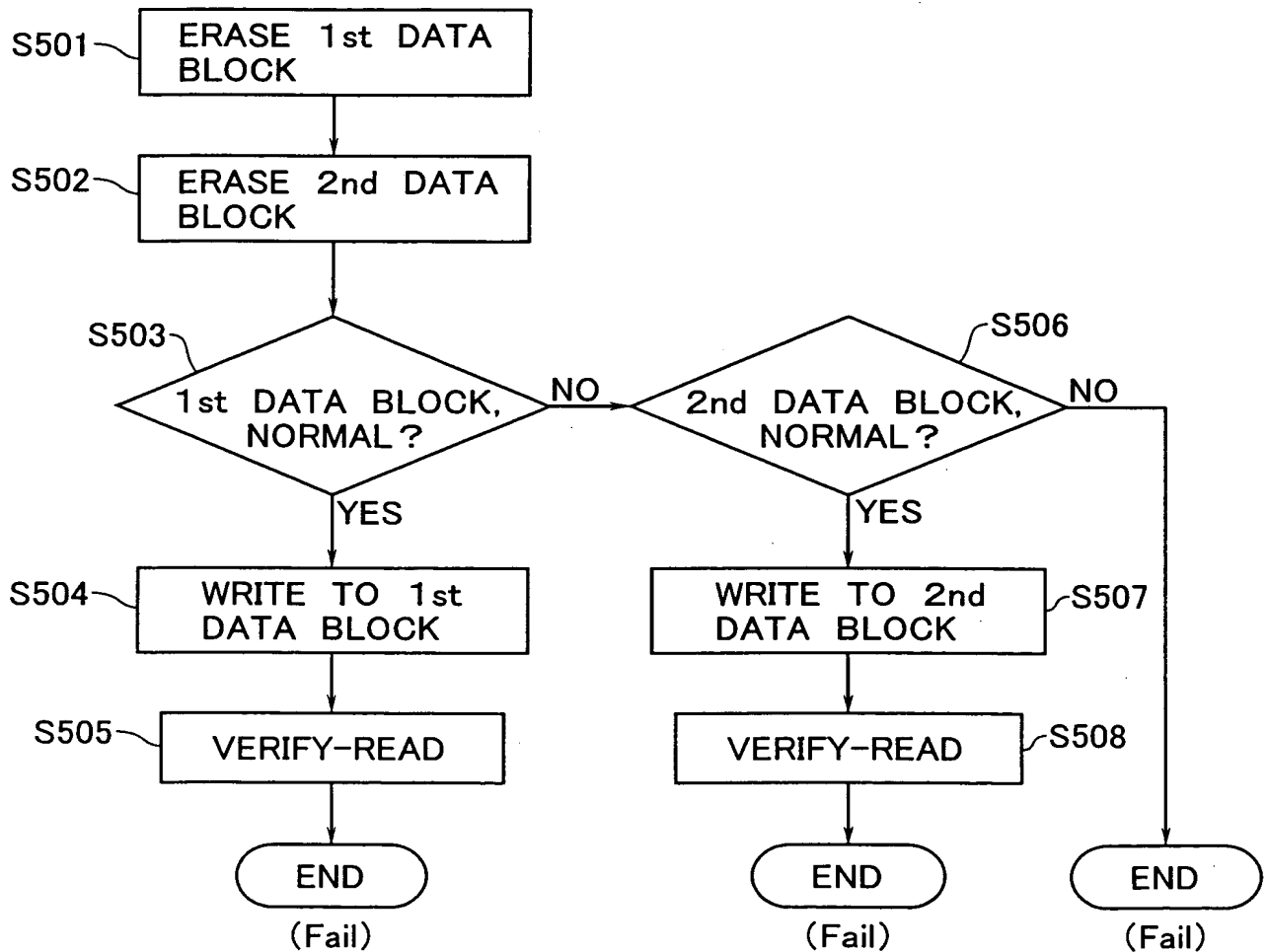


FIG.17

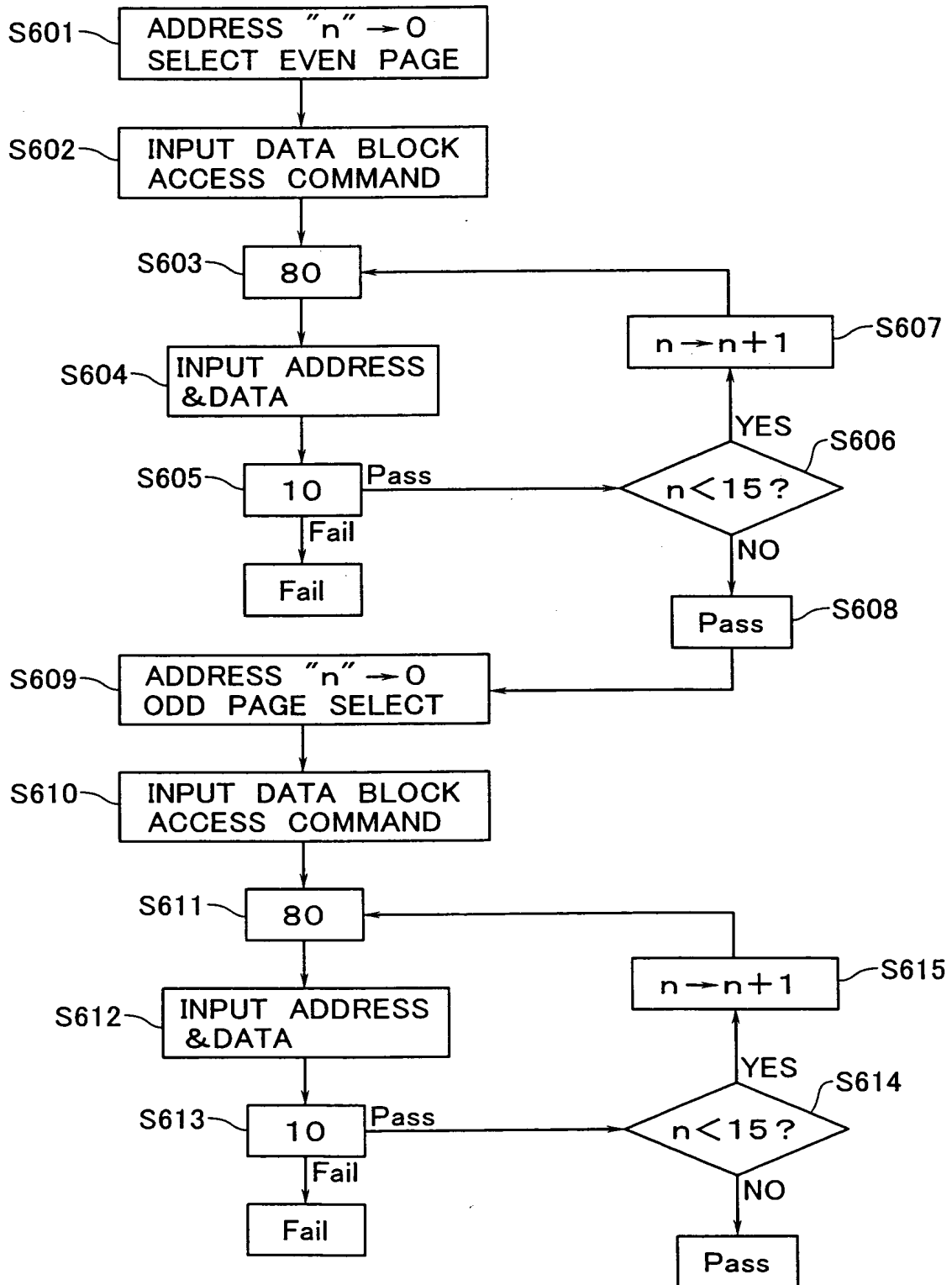
DATA BLOCK WRITE AT S504 & S507



FIG.18

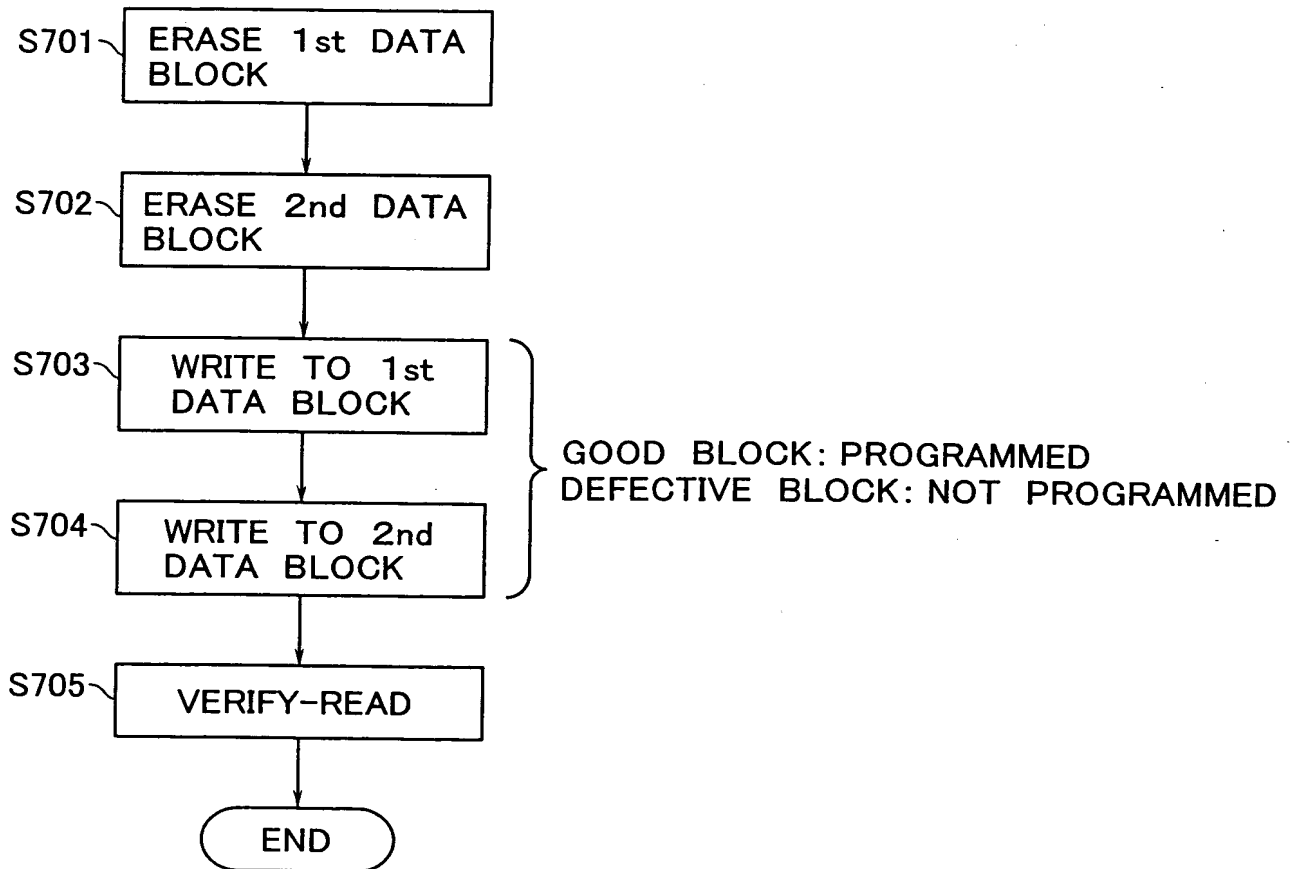
INITIAL SETUP DATA PROGRAMMING  
(WITH AUTOMATIC TEST)

FIG.19

DATA BLOCK WRITING S703 & S704